LISTING OF CLAIMS:

The following listing of claims replaces all previous versions and listings of claims in the present application.

1. (Currently amended) A microcomputer comprising:

a central processing unit (CPU) which operates depending on programs to output a stop command when it stops operation thereof;

a main-clock generating means for generating a main-clock to operate the CPU;

a sub-clock generating means for generating a sub-clock of the frequency which is lower than the main-clock;

an intermittent operation control means which operates by receiving the sub-clock to control the intermittent operation of the CPU and ~~moreover~~ stops, upon reception of the stop command, operation of the main-clock generating means and starts measurement of the predetermined setting time and ~~moreover~~ starts again, after the setting time has passed, operation of the main-clock generating means to raise the CPU to the operating condition from the stop condition in view of realizing the intermittent operation of the CPU; and

an intermittent time measuring means which operates to measure an intermittent time which is a substantial pause period of the CPU,~~by receiving the sub-clock to measure the period in which the CPU is in the stop condition by reading such measured value~~

wherein the CPU is configured to:

read the intermittent time measured by the intermittent time measuring means;

measure, using its own software process, an operation time in which the CPU is in the operating condition; and

measure a total time from a start time of the intermittent operation of the CPU by accumulating the intermittent time and the operation time.

2. (Original) A microcomputer according to claim 1, wherein the intermittent time measuring means is structured to be set, with an operation mode switching command from the CPU, to any operation mode of a first mode to measure a period in which the CPU is in the stop condition and a second mode to continuously measure the time and to clear the measured value with a clear command from the CPU when at least the operation mode is set to the second mode.

3. (Currently amended) A microcomputer comprising:

a CPU which can operate depending on programs and can stop the operation thereof with execution of ~~the~~a predetermined instruction;

a main clock generator generating a main clock to operate the CPU;

a sub-clock generator generating a sub-clock of a lower frequency than the main clock;

an intermittent operation controller which operates by receiving the sub-clock to control the intermittent operation of the CPU and stops, upon reception of a stop command, operation of the main clock generator and starts a measurement of a predetermined setting time and moreover starts again, after the predetermined setting time has passed, operation of the main-clock generator to raise the CPU to the operation condition from the stop condition in view of the realizing the intermittent operation of the CPU;

a level detecting circuit reading and determining, when the CPU is in the stop condition, a level of a monitor object signal supplied to a predetermined input terminal of the microcomputer in every constant period and then raising the CPU to the operating condition from the stop condition when the determined level reaches a particular level;~~,~~ and

~~further comprising:~~

an automatic signal reading means for reading and determining, when the CPU is in the stop condition, a level of the monitor object signal supplied to the predetermined input terminal of the microcomputer in every constant period and then raising the CPU to the operating condition from the stop condition when the determined level reaches the particular level,

wherein the intermittent operation controller starts the operation of the main-clock generator and the CPU even in the case where a rise request is issued from the level detecting circuit during the measurement of the predetermined setting time.

4. (Original) A microcomputer according to claim 3, wherein the automatic signal reading means updates the determined level of the monitor object signal to the level read this time only when the level read from the input terminal becomes identical continuously for a plurality of predetermined times.

5. (Original) A microcomputer according to claim 4, wherein the automatic signal reading means can be switched to an operation mode for executing a filter process depending on a command from the CPU and an operation mode for setting the level read from the input

terminal as the determined level of the monitor object signal without execution of the filter process.

6. (Original) A microcomputer according to claim 3, wherein the particular level is set by the CPU in the automatic signal reading means.

7. (Original) A microcomputer according to claim 3, wherein the constant time is set by the CPU in the automatic signal reading means.

8. (Original) A microcomputer according to claim 3, wherein the automatic signal reading means outputs from the predetermined output terminal of the microcomputer, before reading a level of the monitor object signal from the input terminal, a power feeding signal to supply a voltage to a pull-up resistor for pulling up a signal line for supplying the monitor object signal to the input terminal and stops output of the power feeding signal when the level of the monitor object signal is read from the input terminal.

9. (Original) A microcomputer according to claim 8, wherein a waiting time until level reading of the monitor object signal from output of the power feeding signal is set by the CPU in the automatic signal reading means.

10. (Original) A microcomputer according to claim 8, wherein the automatic signal reading means can be set, depending on a command from the CPU, to an operation mode in which the power feeding signal output control is not executed.

11. (Original) A microcomputer according to claim 3, wherein an input terminal with which the automatic signal reading means reads a signal level is set by the CPU to any one of a plurality of terminals of the microcomputer.

12. (Original) A microcomputer according to claim 3, further comprising a timer rise control means for starting, upon reception of an operation request from the CPU, measurement of time which is previously set by the CPU and then raising the CPU, when such preset time has passed, to the operating condition from the stop condition.

13. (Original) A microcomputer according to claim 3, wherein the automatic signal reading means comprises a read result storage section which stores the level of the monitor object signal determined therewith and allows the CPU to read the stored content.

14. (Original) A microcomputer according to claim 13, wherein the automatic signal reading means can operate with a command from the CPU while the CPU is in the operating condition.

15. (Currently amended) A microcomputer which cooperates with an external apparatus to be driven by a drive signal, comprising:

a CPU to execute the process in relation to the external apparatus;

a main clock generator generating a main clock to operate the CPU;

a sub-clock generator generating a sub-clock of a lower frequency than the main clock;

an intermittent operation control means for controlling intermittent operation of the CPU, by receiving the sub-clock to control the intermittent operation of the CPU and stops, upon reception of a stop command, operation of the main clock generator and starts a measurement of a predetermined setting time and moreover starts again, after the predetermined setting time has passed, operation of the main-clock generator to raise the CPU to the operation condition from the stop condition in view of realizing the intermittent operation of the CPU; and

a timer interlocking control means receiving the sub-clock to operate, and for outputting the drive signal to the external apparatus depending on the ~~preset~~predetermined setting time.

16. (Original) A microcomputer according to claim 15, wherein the intermittent operation control means operates by receiving a sub-clock in the frequency lower than that of a main-clock for operating the CPU.

17. (Original) A microcomputer according to claim 15, wherein the timer interlocking control means operates by receiving the sub-clock in the frequency lower than that of the main-clock for operating the CPU.

18. (Original) A microcomputer according to claim 15, wherein the setting time is set for the timer interlocking control means while the CPU is in the operating condition.

19. (Original) A microcomputer according to claim 15, wherein the setting time is set enough for the external apparatus to complete preparation for process when the CPU rises to the operating condition from the stop condition.